# MONOLITHIC OPTOELECTRONIC RECEIVER FOR Gbit OPERATION

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## Abstract

A monolithic optoelectronic receiver chip was designed and fabricated for operation at 1.0 Gbit/sec data transmission rate. The major components of the receiver chip are a fast photodiode, a preamplifier, and a 1:4 demultiplexer circuit fabricated on semi-insulating GaAs substrate. Optical/electrical functionality has been demonstrated at wafer level.

Optical interconnects provide a means for the practical realization of high data rate communication systems which are either impossible or impractical to implement electrically. As with any other data transmission system, the primary components are a transmitter, a transmission channel, and a receiver. In order to realize the full performance advantages of optical interconnects, optical components are being monolithically integrated with electronic circuitry for the fabrication of transmitters and receivers. With such integration, the parasitic reactance would be much lower than with a hybrid connection. In addition, there would be fewer parts to package, and reduction in the number of wirebonds should result in increased reliability. In this paper, we describe a monolithic optoelectronic receiver chip designed for operation at 1.0 Gbit/sec data transmission rate.

Previous published works[1,2] from this laboratory describing a monolithic transmitter which involved the integration of a semiconductor laser with a 4:1 multiplexer (36 gates) have addressed the problems of integration of optical components (e.g., lasers) with electronic circuitry. Honeywell's approach for the fabrication of the integrated receiver does not require any epitaxial growth for the optoelectronic component (detector), thus bypassing some of the inherent problems of integration. The wafer is fully compatible with the planar IC processing techniques and extendible to electronics of arbitrary size and complexity.

The integrated receiver chip has a single fiber optic input and four electrical outputs. The major components of the receiver chip are: a fast photodiode, a preamplifier circuit, and a 1:4 demultiplexer circuit. All components are fabricated on a semi-insulating GaAs substrate using direct ion implantation MESFET technology. A photograph of the integrated receiver chip is shown in Figure 1. It should be noted that the photodetector takes only a small portion of the surface, the remainder being available for GaAs electronics.

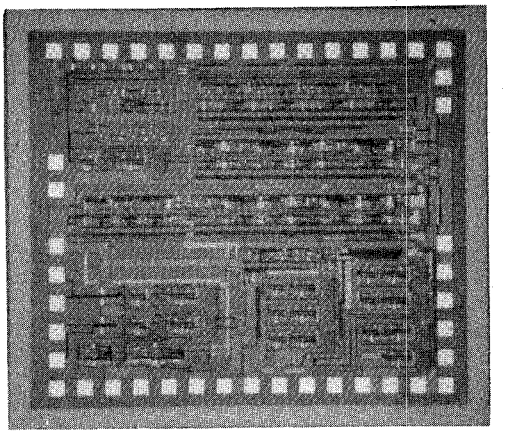

Figure 1. Photograph of the integrated receiver chip

The fast photodetector for the receiver is a back-to-back Schottky photodiode fabricated directly on the semi-insulating substrate. This eliminates the need for epitaxial growth, thus simplifying the fabrication process significantly. Figure 2 shows a pulse response of the back-to-back Schottky photodiode for a bias voltage of -15V. The rise and fall times of the detector response observed for a range of bias voltages between -10V and -15V were under 100 ps. This exceeds the requirements for 1.0 Gbit/sec operation of the receiver chip. The detector output of 0.2 Amp for 1 watt of incident light power at $\lambda = 0.84$ $\mu$m was sufficient to drive the preamplifier stage and generate voltage swings consistent with GaAs logic levels for Honeywell's depletion-mode GaAs digital electronics.

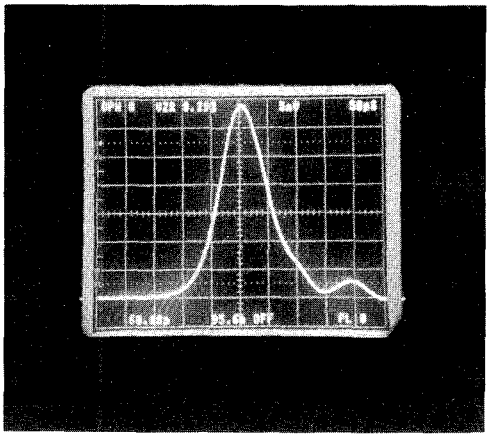

Figure 2. Pulse response of back-to-back Schottky photodiode for bias voltage of -15V.

A number of different preamplifiers were designed and tested for suitability. The preamplifier designs, which included both high impedance and transimpedance types of architecture, underwent extensive computer simulation prior to fabrication. High-speed testing of the preamplifier has not yet been completed. Low-speed testing has shown a voltage gain of 22 dB in the design chosen for integration.

The optical receiver circuit was designed to decode a 1.0 Gbit optical input signal into four parallel 250 Mbit electrical outputs. The key component for this operation is the 1:4 demultiplexer circuit. The DMUX architecture uses a unique SDFL NOR gate logic. The architecture is a scaled down version of Honeywell's 1:8 DMUX which has been operated at clock rates higher than 2.0 GHz. The total number of gates in our current DMUX circuit is 150. The functionality of the different components of the receiver, including the DMUX, was demonstrated by both electrical and optical testing. An optical fiber, coupled at one end to a semiconductor laser, was used for the inputs to the integrated detector. The receiver chip was found to be 100% functional with optical input at low speeds. Currently, a high-speed package is being developed for performing high-speed testing of the receiver at its intended operational speed of 1.0 Gbit/sec.

The monolithic receiver chip described here represents the first reported integration of MSI level (150 gates) electronic circuit with an optoelectronic component. It is a significant step towards realizing the data channels of tremendous capacity needed for the optical interconnect systems of tomorrow.

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References:

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2. "Integrated Optoelectronic Transmitter", J.K. Carney, M.J. Helix, R.M. Kolbas, S.A. Jamison, and S. Ray, SPIE Integrated Optics III, Washington D.C., 1983 Proceedings, 408.